THIN FILM TRANSISTOR ARRAY SUBSTRATE, ORGANIC LIGHT-EMITTING DISPLAY APPARATUS AND METHOD OF MANUFACTURING THE THIN FILM TRANSISTOR ARRAY SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to and the benefit of Korean Patent Application No. 10-2013-0133831, filed on Nov. 5, 2013 in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference.

BACKGROUND

1. Field

Aspects of one or more embodiments of the present invention relate to a thin film transistor array substrate, an organic light-emitting display apparatus, and a method of manufacturing the thin film transistor array substrate.

2. Description of the Related Art

A thin film transistor array substrate including thin film transistors, capacitors, and wiring connecting the thin film transistors and the capacitors is widely used in flat display apparatuses, such as liquid crystal display apparatuses or organic light-emitting display apparatuses. An organic light-emitting display apparatus including the thin film transistor array substrate defines each pixel by arranging a plurality of gate lines and data lines in a form of a matrix. Each pixel includes a thin film transistor, a capacitor, and an organic light-emitting device connected to the thin film transistor. The organic light-emitting device emits light by receiving an appropriate driving signal from the thin film transistor and the capacitor. Thus, a desired image may be displayed.

SUMMARY

One or more embodiments of the present invention include a light-emitting display apparatus having excellent device characteristics and display quality. Additional aspects will be set forth in part in the description that follows and, in part, will be apparent from the description, or may be learned by practice of the presented embodiments.

According to an embodiment of the present invention, a thin film transistor array substrate is provided. The thin film transistor array substrate includes: a substrate; a bottom gate electrode including a gate area doped with ion impurities and undoped areas on left and right sides of the gate area; an active layer on the bottom gate electrode with a first insulating layer therebetween and including a source contact region, a drain contact region, and an oxide semiconductor region; a top gate electrode on the active layer with a second insulating layer therebetween; and a source electrode in contact with the source contact region and a drain electrode in contact with the drain contact region, the source electrode and the drain electrode being on the top gate electrode with a third insulating layer therebetween. The oxide semiconductor region is between the source contact region and the drain contact region.

The gate area may not overlap the source contact region or the drain contact region.

The bottom gate electrode and the top gate electrode may be connected to each other.

The bottom gate electrode may include amorphous silicon or poly silicon.

A thickness of the first insulating layer or the second insulating layer may be less than or equal to a thickness of the third insulating layer.

A thickness of the top gate electrode may be greater than or equal to a thickness of the source contact region or the drain contact region.

A length of the oxide semiconductor region may be less than or equal to a threshold value.

The oxide semiconductor region may include at least one oxide selected from gallium indium zinc oxide (G-I—Z—O), zinc (Zn), indium (In), gallium (Ga), tin (Sn) cadmium (Cd), germanium (Ge), hafnium (Hf), or a combination thereof.

According to another embodiment of the present invention, an organic light-emitting display apparatus is provided. The organic light-emitting display apparatus includes: a first transistor including a bottom gate electrode, a first active layer including a contact region and an oxide semiconductor region, a top gate electrode, a first source electrode, and a first drain electrode; a second transistor including a second active layer of a same layer and of a same material as the bottom gate electrode, a gate electrode of a same layer and of a same material as the contact region, and a second source electrode and a second drain electrode of a same layer and of a same material as the first source electrode and the first drain electrode; and a light-emitting device including a pixel electrode, an interlayer, and a counter electrode. The oxide semiconductor region is between a source contact region and a drain contact region of the contact region. A region of the bottom gate electrode not overlapping the source contact region or the drain contact region is doped with ion impurities.

The bottom gate electrode may include a gate area of a silicon semiconductor and doped with ion impurities, and undoped areas on left and right sides of the gate area.

The first transistor may be a driving transistor of the organic light-emitting display apparatus. The second transistor may be a switching transistor of the organic light-emitting display apparatus.

The first source electrode and the first drain electrode may not overlap the doped region of the bottom gate electrode.

The organic light-emitting display apparatus may further include a capacitor. The capacitor may include a first electrode of the same layer and of the same material as the contact region, and a second electrode of a same layer and of a same material as the top gate electrode.

The capacitor may further include a third electrode of the same layer and of the same material as the first source and first drain electrodes.

The bottom gate electrode may include amorphous silicon or poly silicon.

The second transistor may include an auxiliary gate electrode of a same layer and of a same material as the top gate electrode.

In yet another embodiment of the present invention, a method of manufacturing a thin film transistor array substrate is provided. The method includes: patterning a silicon layer formed on a substrate to form a bottom gate electrode; forming a first insulating layer on the patterned silicon layer; patterning a first conducting layer formed on the first insulating layer to form a source contact region and a drain contact region; doping ion impurities on the bottom gate electrode using the source contact region and the drain contact region as a mask; patterning an oxide semiconductor layer formed on the first conducting layer to form an oxide semiconductor region between the source contact region and the drain contact region; forming a second insulating layer on the patterned first conducting layer and the patterned oxide semiconductor layer; forming a top gate electrode on the second insulating